

# PACKAGE HAVING ARRAY OF METAL PEGS LINKED BY PRINTED CIRCUIT LINES

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## BACKGROUND OF THE INVENTION

### Field of Invention

The present invention relates to a semiconductor package structure and its method of manufacture. More particularly, the present invention relates to a package structure having an array of metal pegs each linked by a printed circuit line to a silicon  
10 chip.

### Description of Related Art

In the semiconductor industry, integrated circuits (ICs) are generally manufactured in three separate stages. First, the semiconductor substrates or silicon wafers are formed using an epitaxial technique. Next, various semiconductor devices  
15 such as MOS transistors and multi-level interconnects are formed in the semiconductor substrate. Finally, the silicon wafers are diced up to form separate dies and then packaged. The purpose of packaging is to provide the necessary protection of the die and the connection to a printed circuit board (PCB) or other electrical component.

Usually, for an IC module, a large number of connections are necessary to link  
20 up a die. Consequently, hundreds of circuit lines are needed to complete the connections. In conventional packages, a lead frame is used to connect the bonding pads on a die with external contact points outside the package. Due to the rapid increase in the level of integration of integrated circuits without a corresponding increase in size of the package, the conventional lead frame type of package is simply

overwhelmed by the number of conductive wires necessary for connection. In addition, electronic products must get lighter, thinner, shorter and smaller with each upcoming generation so that they can be competitive in the marketplace. Hence, new types of packaging techniques such as chip scale package, chip size package and multi-chip module have been developed.

Nowadays, techniques for manufacturing integrated circuits having a line width smaller than 0.18 microns is available. With many breakthroughs in the level of circuit integration, the size of a package has to be minimized as well.

A conventional package uses a lead frame as a die carrier with leads protruding from the side of the package. Because these leads are distributed around the edges of the package, the package has to occupy a larger area. Furthermore, the high lead count limits the distance of separation between neighboring leads or alternatively sets up a lower boundary for the minimum area of a package. Consequently, area array package structures are invented. The contact points of an area array package are usually laid on the bottom surface of the package. For example, ball grid array (BGA), small outline no-lead (SON) and ball chip carrier (BCC) are all area array packages.

Figs. 1A through 1E are cross-sectional views showing the progression of manufacturing steps in fabricating a conventional ball grid array type of die carrier package. First, as shown in Fig. 1A, a photoresist material is deposited over surfaces 102a and 102b of a copper substrate 100 to form photoresist layers 104a and 104b, respectively. Next, the photoresist layer 104a is exposed and developed to form ball lead areas 106 that expose a portion of the surface 102a of the copper substrate 100.

Next, as shown in Fig. 1B, a wet etching operation is conducted, etching the copper substrate 100 using the photoresist layers 104a and 104b as a mask, thereby

forming hemispherical cavities 108 in the ball lead areas 106. Thereafter, an electroplating operation is carried out to form a layer of metallic film 110 over the surface of the hemispherical cavities 108.

Next, as shown in Fig. 1C, both photoresist layers 104a and 104b are removed, and then a die 112 is bonded onto the surface 102a. After that, metallic wires 114 are bonded using a wire bonding machine, thereby linking the bonding pads (not shown in the figure) on the die 112 with the metallic film 110 inside the cavities 108 (Fig 1B).

Next, as shown in Fig. 1D, the upper surface 102a of the copper substrate 100 is sealed off using plastic material such as epoxy 116. The epoxy 116 encloses the die 112, the metallic wires 114 and the metallic film 110 inside the cavity 108 (Fig 1B).

Next, as shown in Fig. 1E, another wet etching operation is carried out to remove the copper substrate 100 entirely (portions labeled 100 in Fig. 1D). Ultimately, the hemispherical metal films 110, the bottom portion of the die 112 and the epoxy 16 are all exposed forming a complete ball grid array type of die carrier package. This type of die carrier package utilizes the hemispherical metallic films 110 as leads for connecting with external circuits.

However, the aforementioned die carrier package has intrinsic reliability problems as well as production yield problems. Since the package uses a metallic film that is made using precious metal as a connecting lead, the metallic film must not be too thick. Yet, saving metal in plating the metallic film makes the film vulnerable to scratches or peelings during transition or transportation. Too much damage to the metallic film is liable to cause a bad connection with a printed circuit board and may ultimately lead to reliability problems when the package is finally mounted using surface mount technology (SMT). Consequently, product yield decreases.

In light of the foregoing, there is a need to provide a method for manufacturing a better type of area array package.

## SUMMARY OF THE INVENTION

5       Accordingly, the purpose of the present invention is to provide a type of package with an array of metal pegs connected by printed circuit wires. The metal pegs can be arranged to form an area array serving as contact points of the package. This type of package structure has a smaller overall thickness. Furthermore, bottom of the die pad is exposed so that heat can be dissipated from the die more readily.  
10       Furthermore, the end face of the metal pegs is electroplated so that the metal pegs can have good bondability, molding compound characteristic and solderability.

      The invention also provides a method of forming a package structure having an array of metal pegs connected by printed circuit lines. The method is capable of producing high yield and high reliability packages such that surface mount technology  
15       can be readily applied.

      To achieve these and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, the invention provides a package structure having an array of metal pegs connected by printed circuit lines. Structurally the package includes a die pad having a silicon die on top. The underside of the  
20       package contains a plurality of external metal pegs arranged to form an area array. Surrounding the die near the edge of the package is a number of internal metal pegs that are electrically connected to various bonding pads on the die. The die, the die pad, and the internal metal pegs are all sealed off using insulating material so that only the bottom portion of the die pad is exposed. Each external metal peg can be electrically

connected to an internal metal peg via a printed circuit line. Moreover, the end face of each internal or external metal peg contains an electroplate layer.

In another aspect, this invention provides a method for forming a package having an array of metal pegs connected by printed circuit lines. The method includes

5 the steps of providing a metal substrate, and then forming electroplated layers in the metal peg areas on both the upper and lower surface of the metal substrate. Next, photoresist layers are formed on the upper and lower surface of the metal substrate. The photoresist layers cover the non-electroplated area on the lower surface of the metal substrate as well as the desired area for forming die pad on the upper surface of the

10 metal substrate. Thereafter, the upper surface of the metal substrate is etched to remove a portion of the substrate material to form a die pad and internal metal pegs. After removing the photoresist layers, a silicon die is attached to the die pad. Then, electrical connections are made between the die and the internal metal pegs. Subsequently, insulating material is used to seal off the die, the die pad and the internal

15 metal pegs. Next, a circuit line mask is formed inside the printed circuit line region on the lower surface of the metal substrate. Then, an etching operation is conducted to expose a portion of the insulating material and the bottom part of the die pad as well as to form external metal pegs and printed circuit lines. Each printed circuit line is used as a medium for linking each internal metal peg to an external metal peg.

20 It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

## BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention. In the drawings,

Figs. 1A through 1E are schematic, cross-sectional views showing the progression of manufacturing steps for fabricating a conventional ball grid array type of die carrier package;

Figs. 2A through 2I are schematic, cross-sectional views showing the progression of manufacturing steps for fabricating a package structure having an array of metal pegs connected by printed circuit lines according to the preferred embodiment of this invention;

Figs. 3A and 3B are the respective top and bottom schematic views of the metal substrate half-way into the steps required to form the package structure according to the method of this invention;

Fig. 4 is a schematic, top view showing a die attached to a die pad of the metal substrate and wire bonded to internal metal pegs according to the method of forming the package structure in this invention;

Fig. 5 is a schematic, top view of the lower surface of the package according to this invention after a circuit line mask is formed over the metal substrate for a first type of external metal peg arrangement;

Fig. 6 is a schematic, top view of the lower surface of the package according to this invention after a circuit line mask is formed over the metal substrate for a second type of external metal peg arrangement;

Fig. 7 is a schematic, perspective view showing a printed circuit line and bonding pad structure of a package fabricated according to the method of this invention; and

Figs. 8A and 8B are schematic, cross-sectional views showing two different structural arrangement of the circuit line mask and the printed circuit line according to the method of forming the package structure in this invention.

### DESCRIPTION OF THE PREFERRED EMBODIMENTS

Reference will now be made in detail to the present preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers are used in the drawings and the description to refer to the same or like parts.

Figs. 2A through 2I are schematic, cross-sectional views showing the progression of manufacturing steps in fabricating a package structure having an array of metal pegs connected by printed circuit lines according to the preferred embodiment of this invention.

First, as shown in Fig. 2A, a metal substrate 200 is provided. The metal substrate 200 can be made from material including copper, iron, copper alloy (C151, C194, C7025, KCF125 or EFTEC) or nickel-iron alloy (Ni-Fe 42 alloy). Next, a layer of photoresist is coated on the first surface 202a and the second surface 202b of the metal substrate 200. After exposure and development of the photoresist layer in photolithographic operations, a first photoresist pattern 204a is formed in a metal peg region 206a on the surface 202a of the metal substrate 200. Similarly, a second

photoresist pattern 204b is formed in another metal peg region 206b on the surface 202b of the metal substrate 200.

As shown in Fig. 2B, electroplating is carried out to form electroplate layers 208a in the metal peg region 206a and electroplate layers 208b in the metal peg region 206b of the metal substrate 200. The electroplate layers 208a and 208b can be made from material including gold (Au), silver (Ag), nickel (Ni), palladium (Pd), nickel-palladium alloy (Ni-Pd alloy) or a composite layer composed of a combination of different materials. Preferably, the electroplate layer is formed by first plating a layer of nickel, then plating a layer of nickel-palladium layer on top, and finally plating a layer of palladium. The purpose of having a nickel layer is to prevent corrosion, and the purpose of having a palladium layer is to enhance bondability, molding compound characteristic and solderability.

As shown in Fig. 2C, the photoresist layers 204a and 204b are removed. Thereafter, photoresist material is again deposited over the surfaces 202a and 202b of the metal substrate 200. After the photoresist material is exposed and developed, patterned photoresist layers 210a and 210b are formed. The photoresist layer 210b on the surface 202b covers the area not protected by the electroplate layers 206b. The photoresist layer 210a on the surface 202a, on the other hand, covers and thus marks out the desired die pad area 236.

Figs. 3A and 3B are the respective top and bottom views of the metal substrate half-way into steps required to form the package structure according to the method of this invention. As shown in Figs. 3A and 3B, a number of packages can be produced simultaneously on the same piece of metal substrate. Fig. 3A is a top view of the metal substrate, which is the same view seen when looking at the surface 202a in Fig.



2C. The photoresist layer 210a over the die pad area is located in a central position, and the electroplate layers 208a are located in the region that surrounds the die pad area. Fig. 3B is a bottom view of the metal substrate, which is the same view seen when looking at the surface 202b in Fig. 2C. The electroplate layers 208b are arranged to  
5 form an area array pattern on the surface 202b. The remaining areas on the surface 202b not covered by the electroplate layers 208b are covered by the photoresist layer 210b.

Each electroplate layer 208a shown in Fig. 3A is rectangular, but each electroplate layer 208b shown in Fig. 3B is circular. These particular shapes are  
10 chosen for illustration only. In fact, the electroplate layers 208a and 208b can be fabricated into any convenient geometric shape.

As shown in Fig. 2D, using the photoresist layers 210a and 210b as well as the electroplate layers 208a and 208b as an etching mask, a half-etching operation is carried out. During the half-etching operation, a portion of the metal substrate material on the  
15 portion of the surface 202a is removed to form a die pad 212 and a number of metal pegs 214 in the surrounding area.

As shown in Fig. 2E, the photoresist layers 210a and 210b are removed. Thereafter, a silicon die is attached to the die pad 212 and then electrical connection is made between the metal pegs 214 and the bonding pads on the die. The die 220 can be  
20 fixed onto the upper surface 216a of the die pad 212 using bonding material 218 such as insulating glue, conductive glue or tapes. Electrical connections between the electroplate layer 208a on the metal pegs 214 and bonding pads (not shown) on the die can be made using conductive wires 222, for example, in a wire bonding machine. The conductive wires 222, for example, can be gold or aluminum wires.

Fig. 4 is a top view showing a die attached to a die pad of the metal substrate and wire bonded to internal metal pegs according to the method of forming the package structure in this invention. As shown in Fig. 4, the die pad 212 for carrying the die 220 has an area smaller than the die 220. The connection between each bonding pad on the die 220 and each electroplate layer 208a is made by bonding conductive wires 222 such as gold or aluminum wires using a wire bonding machine.

As shown in Fig. 2F, a molding operation is carried out to enclose the silicon die 220, the die pad 212, the conductive wires 222 and the metal pegs 214 with insulating material 224. The insulation material 224 can be resin or epoxy. The molding operation is carried out only on the surface 202a of the metal substrate 200, and so the surface 202b is free of the insulation material 224.

As shown in Fig. 2G, a circuit line mask 226 is formed on the surface 202b of the metal substrate 200. The circuit line mask 226 is formed using, for example, a screen printing process. The screen printing process includes spreading insulating paint over the desired trace line area, then baking the paint so that it hardens, and finally obtaining an insulating paint layer with a circuit line mask 226. The paint includes any thermally hardened type of insulating paint.

Fig. 5 is a top view of the lower surface of the package according to this invention after a circuit line mask is formed over the metal substrate for a first type of external metal peg arrangement. As shown in Fig. 5, the circuit line mask 226 serves as a mask for forming printed circuit lines on the final package. The printed circuit lines are the necessary media for electrically linking together the electroplate layers 208a and the electroplate layers 208b.

As shown in Figs. 4 and 5, the electroplate layers 208a are distributed around the die. The electroplate layers 208a above the metal substrate 200 are normally arranged so that they correspond in position to the die pads on the die 220. Since the distribution of die pads on the die 220 can have many types of configurations, the distribution of electroplate layers 208a as shown in Fig. 5 should not be used to limit the scope of the invention. Fig. 6 is a top view of the lower surface of the package according to this invention after a circuit line mask is formed over the metal substrate for a second type of external metal peg arrangement.

As shown in Fig. 2H, using the electroplate layers 208b and the circuit line mask 226 as an etching mask, the exposed surface 202b of the metal substrate 200 is etched. During the etching operation, a portion of the metal substrate 200 is removed exposing a portion of the insulating material 224 to form external metal pegs 230 and printed circuit lines 228. Hence, a package having an array of metal pegs connected by printed circuit lines is formed. After the etching operation, the die pad 212 has a profile with its lower surface 216b at the same level as the underside of the package. The metal external metal pegs 230 are electrically connected to the internal metal pegs 214 via the printed circuit lines 228. Alternatively, the external metal pegs 224 and the internal metal pegs can be electrically connected directly without the need of a circuit line.

As shown in Fig. 2H, the package structure of this invention includes at least a die pad 212 with a silicon die 220 on its upper surface 216a. The lower surface 216b of the die pad 212 is exposed. The external pegs 230 are positioned around the die pad 212 area forming an area array layout. One end of each internal metal peg 214 is buried inside the insulating material 224 of the package and is electrically connected to

a bonding pad on the die 220. The other end of the metal peg 214 is connected to a printed circuit line 228 so that the internal metal peg 214 is electrically connected to an external metal peg 224 via the circuit line 228. However, an internal metal peg and an external metal peg 228 can also be electrically connected directly. In addition, the end  
5 face of each internal metal peg 214 has an electroplate layer 208a. Similarly, the end face of each external metal peg 224 also has an electroplate layer 208b. These electroplate layers 208a and 208b are convenient locations for carrying out electrical connection, molding and subsequent soldering process.

Fig. 7 is a perspective view showing a printed circuit line and bonding pad  
10 structure of a package fabricated according to the method of this invention. As shown in Fig. 7, the printed circuit line 228 and the bonding pad 234 are connected together. The printed circuit line 228 is covered by the circuit line mask 226, and the upper surface of the bonding pad 234 is covered by the electroplate layer 208b. A cross-section of the printed circuit line 228 and the circuit line mask 226 is shown in Fig. 8A.

Fig. 8B illustrates schematic, cross-sectional views showing a structural  
15 arrangement of the circuit line mask and the printed circuit line that differs from Fig. 8A according to the method of forming the package structure in this invention. As shown in Fig. 8B, sidewall masks 226a are also formed on the sidewalls of the printed circuit line 228. In other words, the printed circuit line 228 is enclosed by the sidewalls  
20 masks 226a and the circuit line mask 226. Therefore, the possibility of damage is lowered while the degree of attachment with the insulating material is increased. The method of forming the sidewall masks 226a is very similar to the method for forming the circuit line mask 226. For example, a screen printing method can be used by first

coating a layer of insulating paint on the sidewalls of the printed circuit line, and then baking to harden the paint.

As shown in Fig. 2I, soldering material 232 can be deposited onto the electroplate layers 208b at the bottom side of the finished package. The soldering material 232 can serve as a medium for the subsequent connection of the IC package with a printed circuit board. The soldering material can be any conductive material such as solder paste, a solder ball or a copper ball. A ball grid array (BGA) structure is formed if a solder or copper ball is attached to each electroplate layer 208b. On the other hand, if solder paste is used, then a land grid array (LGA) structure is formed. Finally, the attached packages are separated using a method similar to separating silicon dies in a wafer.

In summary, major characteristics of this invention include the following:

1. The package of this invention utilizes metal pegs as external leads for connecting a die with external circuits. Since the metal pegs can be arranged to form an area array, level of integration for the package is increased. Furthermore, the metal pegs have better mechanical strength, and so are capable of increasing the reliability as well as the yield of such package.

2. Since a one-sided molding process is used in this invention, package thickness and hence its overall volume is minimized. Furthermore, the lower surface of the die pad is exposed after etching the exposed metal substrate on the bottom side of the package. Hence, the amount of heat dissipated from the die per unit time is increased.

3. The face at one end of the metal peg is covered by an electroplate layer that also serves as an etching mask. The metal pegs can have good bondability, molding

compound characteristic and solderability if proper electroplate material is chosen. Consequently, both product yield and subsequent surface soldering capacity improves.

4. Solder balls or copper balls can be attached to or solder paste can be smeared on the terminal surface of the external metal pegs to form a ball grid array or a land grid array. Hence, the necessary electrical connection to a printed circuit board can be provided.

It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention cover modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.